

Analog Layout Engineer

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Company: Chipright

Location: Netherlands

Category: computer-and-mathematical

Analog Layout Engineer (22nm deep micron CMOS technology)Chipright seeks highly motivated and experienced Analog Layout development engineer to work within a team of highly experienced engineers on 22 nanometer technology.

5+ years' minimum experience in Analog Layout

Experience in High Speed Layout of SERDES

Experience in Layout of blocks such as PLLs, Transceivers, Receivers

Experience working on deep sub-micron CMOS (28nm or less)

Proficient with Synopsys & Cadence tools

Ability to influence the architecture-level and design to ensure design layout can be achieved

Experience with Floor Planning, Power Routing and ESD level design

Experience with Place & Route, Layout Finishing

Experience with Design Rule Checking (DRC) and all aspects of Physical Verification

Experience in working with EDA tool suppliers to yield the best results from their tools

Strong debug & problem-solving skills

Educated to degree level with excellent analytical, communication and documentation skills

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